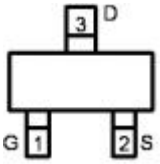
WT3415

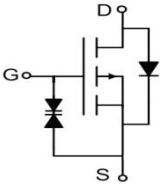
20V P-Channel MOSFET

ID(max)=-4A,
BVDSS=-20V,
RDS(on) =37mΩ @VGS =-4.5V
RDS(on) = 50mΩ @VGS =-2.5V

SOT23



Marking and pin Assignment



Schematic diagram

Features

- Low on-state resistance
- ESD Rating：2500V HBM
- High Power and current handing capability
- Lead free product

General Description

These P-Channel enhancement mode power field effect transistors are produced using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance and gate charge, provide superior switching performance and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for battery protection, load switching, power management and a wide variety of other applications.

Absolute max Ratings(TJ = 25°C unless otherwise noted)

Symbol	Parameter	Units	Maximum
V_{DS}	Drain-Source Voltage	V	-20
V_{GS}	Gate-to-Source Voltage	V	±10
I_D @ TC = 25°C	Continuous Drain Current, VGS @ -4.5V ①	A	-4
I_D @ TC = 100°C	Continuous Drain Current, VGS @ -4.5V ①	A	-3.2
I_{DM}	Pulsed Drain Current②	A	-32
P_D	Power Dissipation①	W	1.39
	Derating Factor①	W/°C	0.011
T_J	Operating Junction Temperature Range	°C	-50 to + 150
T_{STG}	Storage Temperature Range	°C	-50 to + 150

Thermal Characteristics

$R_{\theta JA}$	Maximum Junction-to-Ambient③④	°C/W	90

Electrical characteristics(TJ = 25°C unless otherwise noted)

Symbol	Parameter	Test conditions	Units	Min.	Typ.	Max.
$V(BR)_{DSS}$	Drain-to-Source breakdown voltage	V_{GS} = 0V, I_D =-250μA	V	-20	—	—
$R_{DS(on)}$	Static Drain-to-Source on-resistance	V_{GS}=-4.5V, I_D=-4A	mΩ	—	—	50
		V_{GS}=-2.5V, I_D=-2A	mΩ	—	—	60
		V_{GS}=-1.8V, I_D=-2A	mΩ	—	—	90

		V_{GS}=-1.5V, I_D=-0.8A	mΩ	—	—	110
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D =-250μA	V	-0.35	—	-0.9
I_{DSS}	Drain-to-Source leakage current	V_{DS} =-20V,V_{GS} = 0V	μA	—	—	-1
I_{GSS}	Gate-to-Source forward leakage	V_{GS} =10V	uA	—	—	10
		V_{GS} = -10V		-10	—	—
V_{SD}	Diode Forward Voltage	I_S=-1A, V_{GS}=0V	V	—	—	-1
g_{FS}	Forward Transconductance	V_{DS}=-5V, I_D=-4A	S	4	—	—

Dynamic characteristics(TJ = 25°C unless otherwise noted)

Symbol	Parameter	Test conditions	Units	Min.	Typ.	Max.
C_{iss}	Input capacitance	V_{GS} = 0V V_{DS} = -10V f = 1MHz	pF	—	950	—
C_{oss}	Output capacitance			—	160	—
C_{rss}	Reverse transfer capacitance			—	120	—
Q_g	Total gate charge	VDS=-10V, ID=-4A, VGS=-4.5V	nC	—	12	—
Q_{gs}	Gate-to-Source charge			—	1.4	—
Q_{gd}	Gate-to-Drain("Miller") charge			—	3.1	—
$t_{D(on)}$	Turn-On Delay Time	V_{DD}=-10V, ID=-4A, V_{GS}=-4.5V, R_{GEN}=5Ω	ns	—	12	—
t_r	Turn-On Rise Time			—	10	—
$t_{D(off)}$	Turn-Off Delay Time			—	19	—
t_f	Turn-Off Fall Time			—	25	—
t_{rr}	Body Diode Reverse Recovery Time	I_F=-4A, dI/dt=-100A/μs, T_J =25°C	ns	—	37	—
Q_{rr}	Body Diode Reverse Recovery Charge		nC	—	334	—

① Based on $T_{J(MAX)}$=150°C in a SOT23 package, using junction-to-ambient thermal resistance

② Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C.

③ The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

④ These tests are performed with the device mounted on 1 in2 FR-4 board with 2oz. Copper, in a still air environment with TA=25° C.

Typical electrical and thermal characteristics：

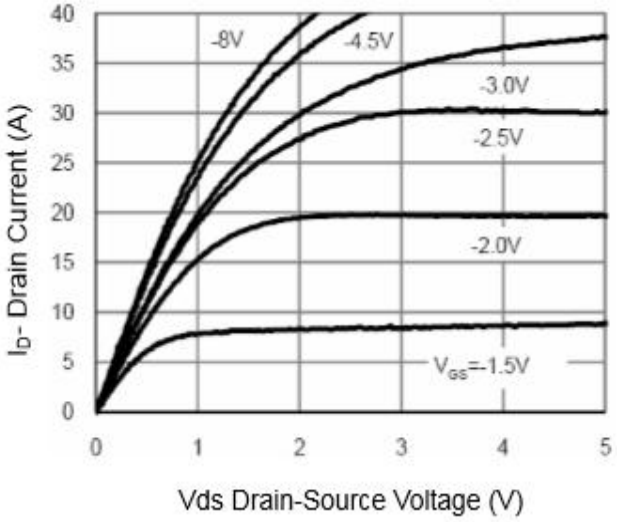


Figure 1: Typical Output Characteristics

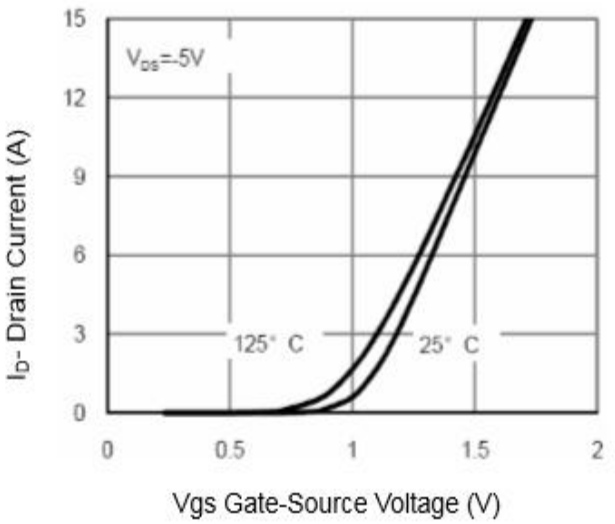


Figure 2: Typical Transfer Characteristics

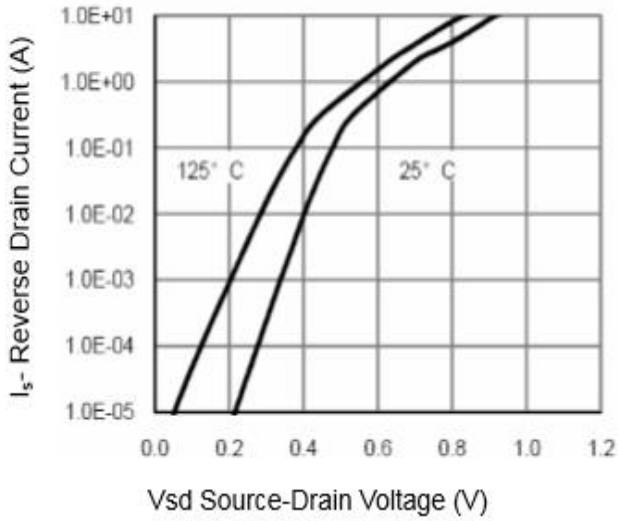


Figure 3: Body-Diode Characteristics

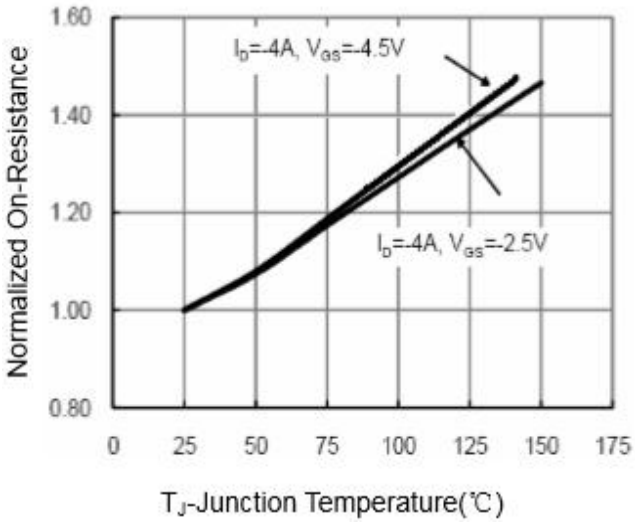


Figure 4: On-Resistance vs. Junction Temperature

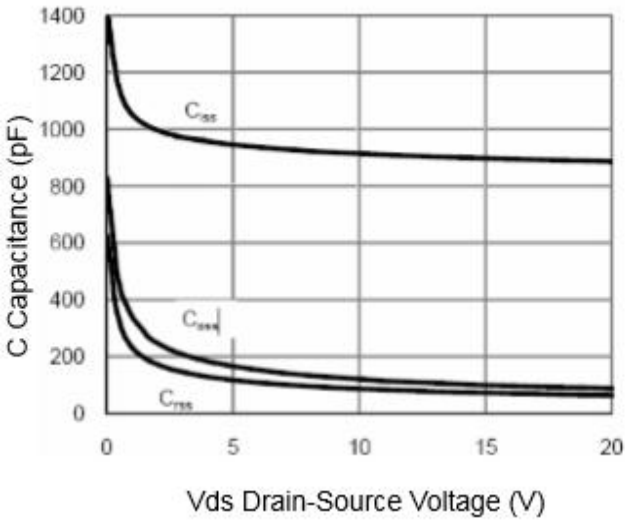


Figure 5: Capacitance Characteristics

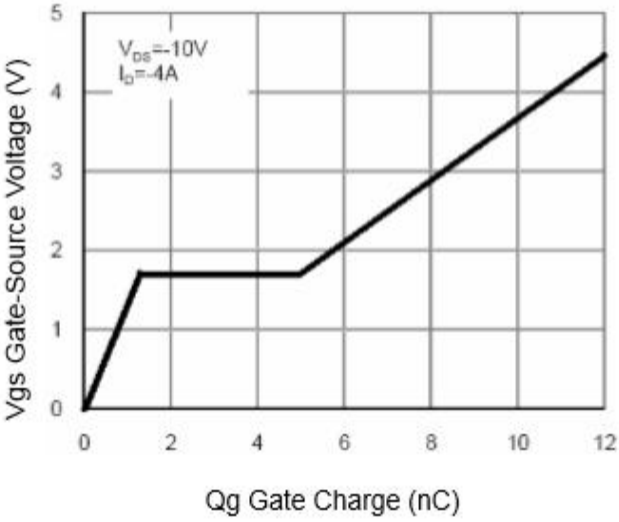


Figure 6: Gate-Charge Characteristics

Typical electrical and thermal characteristics：

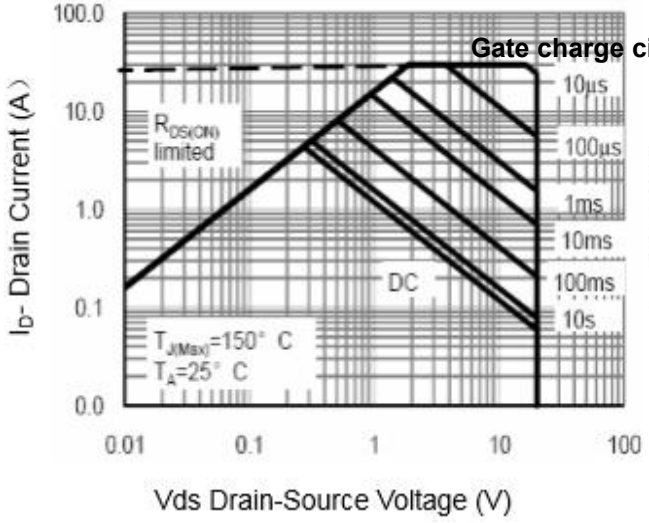


Figure 7: Maximum Forward Biased Safe Operating Area

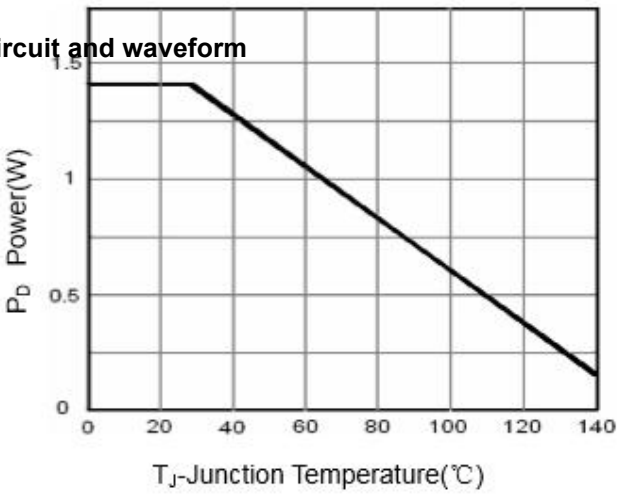


Figure 8: Power Dissipation

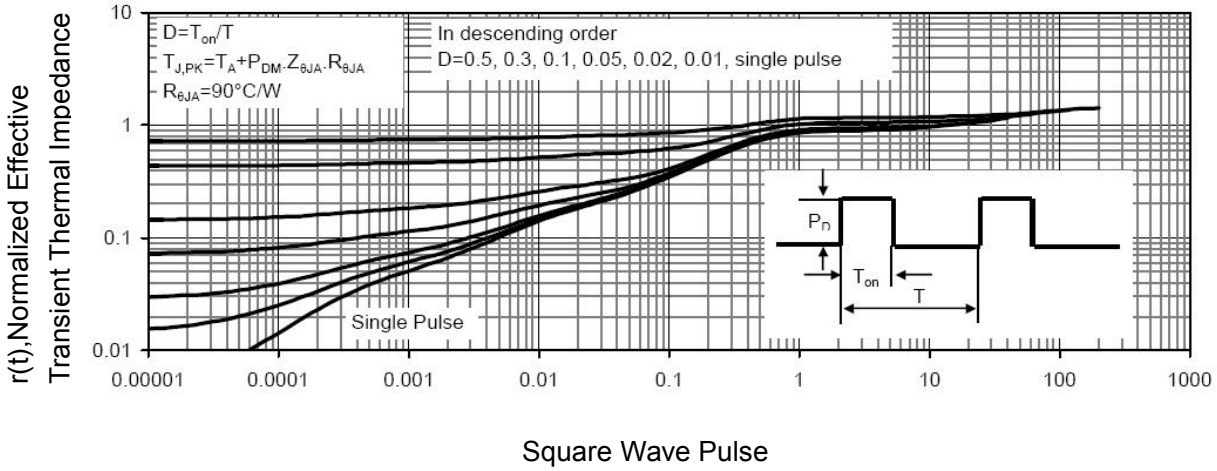


Figure 9: Normalized Maximum Transient Thermal Impedance

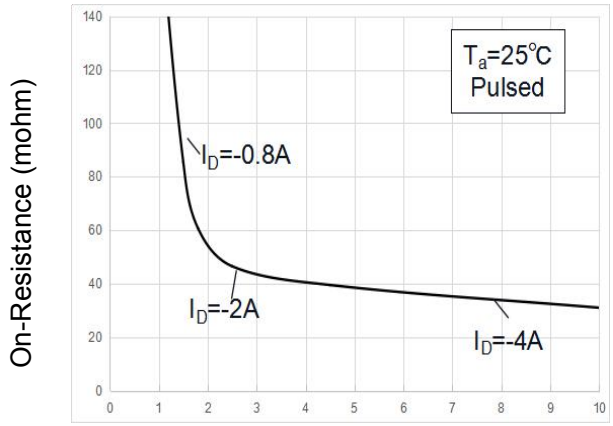
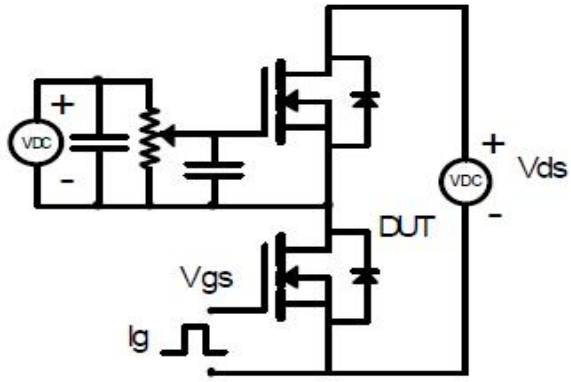
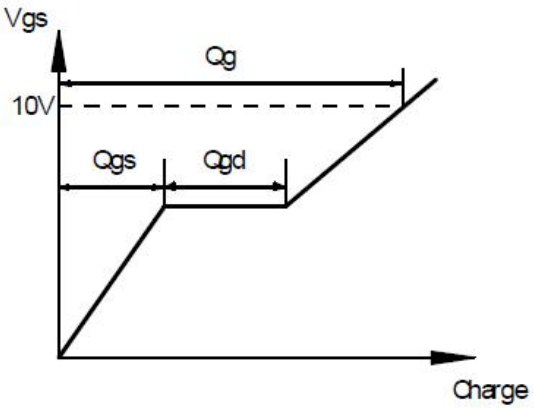


Figure 10: On-Resistance vs. V_{GS}

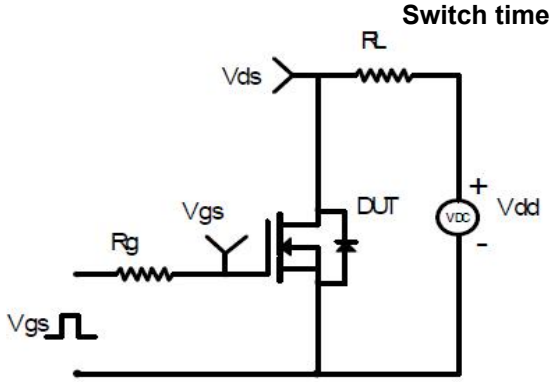
Test circuits and Waveforms:

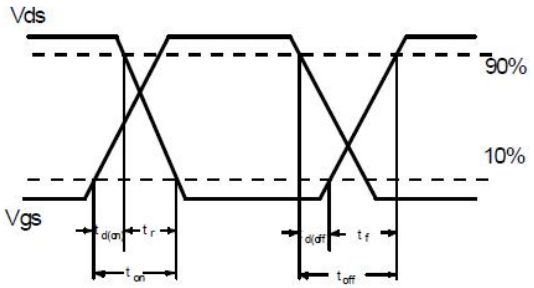
Gate charge circuit and waveform



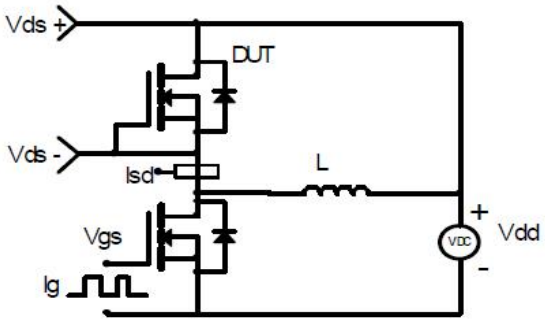


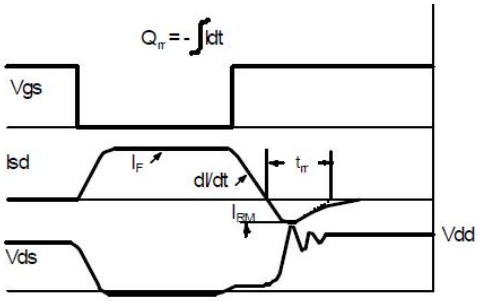
Switch time circuit and waveform



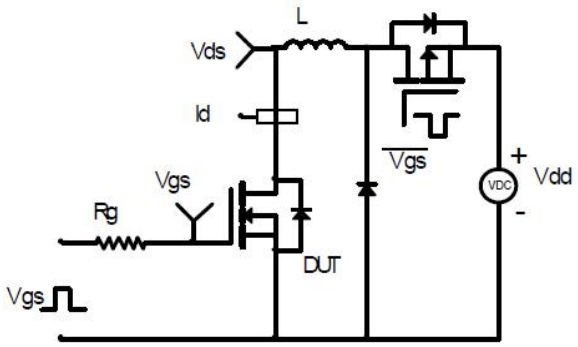


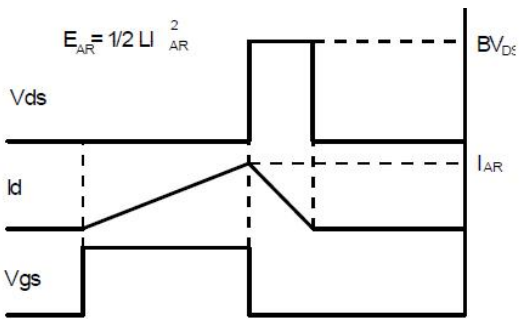
Reverse recovery test circuit and waveform





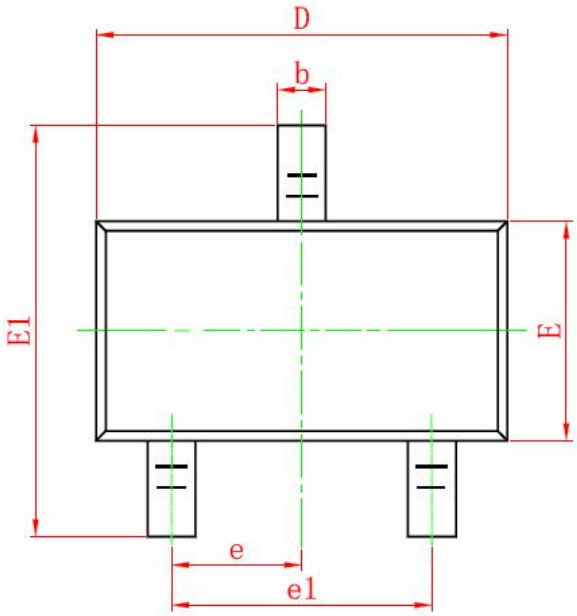
EAS test circuit and waveform

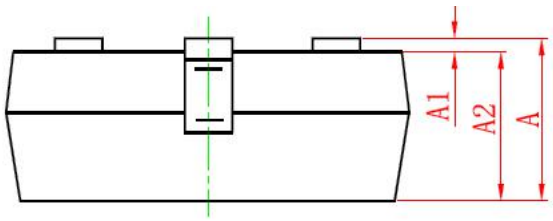


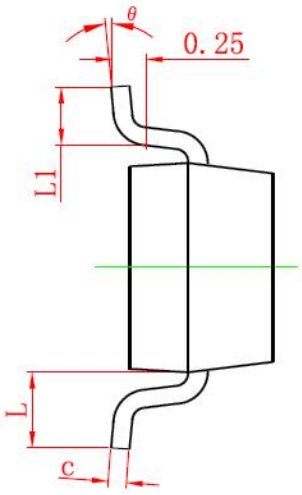


Mechanical Data：SOT23

Dimensions in Millimeters (UNIT:mm)







Symbol	Dimensions in	
	MIN.	MAX.
A	0.9	1.15
A1	0	0.1
A2	0.9	1.05
b	0.3	0.5
c	0.08	0.15
D	2.8	3
E	1.2	1.4
E1	2.25	2.55
e	0.950TYP	
e1	1.8	2
L	0.550REF	
L1	0.3	0.5
θ	0°	8°

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
3415	WT3415	SOT-23	Ø330mm	12mm	3000 units